REMARKS

The Office examined claims 1-15 and rejected each. With this paper, one claim is amended and no claims are cancelled or added, and so claims 1-15 are pending. Asynchronous wrapper claim 1, and method claim 11 are the only independent claims.

Applicants note that the dependent claims were rejected without explanation in a manner inconsistent with the completeness requirements of 37 CFR 1.104(b). Applicants therefore request complete examination in the next Office Action, and Applicants respectfully request that it be made non-final.

Rejection of Claim 11 under 35 USC §112

At p. 2 of the Office Action, independent claim 11 is rejected for usage of the term “possibly.” The claim has been amended so as to obviate the grounds for rejection.

Rejection of Claims under 35 USC §103

At p. 2 of the Office Action, all claims are rejected under 35 USC §103(a) as being unpatentable over US Pat. No. 6,513,128 to Wang et al. (hereinafter Wang), in view of US Pat. No. 6,850,754 to Nakano (hereinafter Nakano).

Applicant respectfully submits the claims are directed to an asynchronous circuit. Page 2, lines 5-9 of the English translation of the present application explains that asynchronous circuits dispense with a time raster with discreet time steps. Driving asynchronous circuits is based on the occurrence of events such as requests received from external circuits, but not on regular clock signals. It should further be noted that the term "wrapper" is known in the art for referring to the asynchronous part of a so-called "globally asynchronous locally synchronous" (GALS) circuit. As explained on page 2, lines 22-29 of the present application, the asynchronous wrapper is for

association with a locally synchronous circuit block. In operation, it is responsible for a conversion of an asynchronous communication of the associated locally synchronous circuit block with an external other locally synchronous circuit block (that has its own asynchronous wrapper). That is, each such locally synchronous circuit block has an asynchronous wrapping circuit, which handles the communication with the outside world, which is any other synchronous circuit block, typically on chip.

The Office appears to rely upon two references from the completely "synchronous world."

Wang relates to a network interface card and comprises means for allowing access to the network interface card also in a low-power mode, i.e. when the computer to which the network interface card is connected, is switched off. To allow access to registers on the network interface card also during power-down of the computer, there is a separate power source and a separate clock signal, referred to as the ASIC clock signal, which are used to access the network interface card during power-down of the computer.

The Office mistakenly identifies the ASIC clock with the pausable clock unit of the asynchronous wrapper of claim 1. The generation of a second clock signal in the event of an applied request signal according to claim 1, is mistakenly identified in the Office action with the regular PCI clock provided to the network interface card during regular operation.

It should be pointed out that the PCI clock signal of Wang is a fully autonomous clock signal which is not generated “in a defined time relationship with” request signals received from outside, as the claims require. The circuit providing the PCI clock is fully synchronous and not at all event-driven. To give an example of the difference between the PCI clock signal and the second clock signal of claim 1, the PCI clock signal would drive the network interface card in an idle state, that is for instance, when no communication request is received at the input side of the network interface card. The second clock signal, in contrast, would not be generated in the

absence of incoming request signals from outside the asynchronous wrapper (except for situations, in which a pipeline must be emptied during some additional clock cycles).

The clock control disclosed by Nakano allows a selection of the clock signal between two different clock oscillators operating at different operating frequencies. This way, interference in wireless communication can be avoided, cf. Nakano col. 4 / col. 5. Again, the mode of operation is completely synchronous for any of the oscillator frequencies used.

A skilled person could not arrive at designing the asynchronous wrapper circuit of claim 1 by a combination of the two synchronous circuits of Wang et al. and Nakano. None of the documents discloses the existence of a defined time relationship between the second clock signal and the request signal in the presence of an applied request signal at the input of the wrapper circuit. None of the documents discloses the suppression of the delivery of the first clock signal to the favor of the delivery of the second clock signal in the event that a request signal is applied at the input. And, almost needless to mention, none of the documents is concerned with an asynchronous circuit.

Notwithstanding the above, at p. 2 of the Office Action, the Office states that Wang teaches:

> an input unit [Fig. 1, clock control 108] which is adapted to receive a request signal [Fig. 1, confReq] from outside and to indicate the reception of the request signal by the delivery of an acknowledgement signal [Fig. 1, configDone].

At p. 3 of the Office Action, the Office further states that:

> [The Wang device is] characterized in that the input unit is adapted to produce, if a request signal is applied, a second clock signal [PCI clock] which is in a defined time relationship with the request signal and to deliver it to the internally synchronous circuit block

> that clock control 108 is not adapted to receive a request signal from outside, it does not indicate the reception of the request signal by the delivery of an acknowledgement signal, nor is it characterized in that the input unit is adapted to produce a second clock signal, all of which are required by the claimed invention.

Clock control 108 receives an internal signal configReq/ configDone from PCI pending handler 105. Signal configReq/ configDone originates from inside the device, not outside. The Office appears to be interpreting “outside” to mean outside the input unit and not outside the asynchronous wrapper. Applicant respectfully submits that this interpretation is incorrect. If “outside” pertained only to the input unit, there would be no point is saying "outside," since anything the input unit receives is from outside the input unit. With this paper, the claims are changed to recite “outside the asynchronous wrapper.”

The Office asserts that signal configDone is sent by clock control 108 to indicate the reception of the request signal. But signal configDone is actually sent by PCI pending handler 105 to clock control 108 when PCI pending handler 105 enters the CONFIG_DONE state, thereby directing clock control 108 to switch the clock back to the ASIC clock if the PC is still in the power down mode. Because signal configDone is not sent by clock control 108 (apparently believed by the Office to be equivalent to the claimed input unit), signal configDone cannot indicate the reception of the request signal.

Clock control 108 *does* output signal PCIClkEn, but signal PCIClkEn does not indicate the reception of the request signal. Rather, signal PCIClkEn is used to indicate switching the clock from one clock source to another. It is not an acknowledgement signal that is dispatched upon receipt of an input signal, rather, it is asserted only when PCIClk is enabled. Because there exist various states in which signal PCIClkEn would not be

asserted (or changed) upon receipt of an input signal, PCIClkEn cannot indicate the reception of the request signal.

Lastly, clock control 108 is not adapted to produce, if a request signal is applied, a second clock signal (or any other clock signal). Clock control 108 produces signal PCIClkEn, which is used as the signal select input by the clock multiplexer. Clock control 108 controls which clock is used; it does not produce a clock signal. According to Wang, both clock signals are generated externally. Signal PCIClk is drawn from the external PCI bus, and asicClk is drawn from an external application specific integrated circuit. Clock control 108 is therefore not adapted to produce, if a request signal is applied, a second clock signal.

Applicants thus submit that even if Wang were modified so as to incorporate Nakano's pausable clock unit in the manner suggested by the Office, the combination of cited references would fail to teach or suggest all elements of claim 1. The same arguments apply to claim 11. Applicants therefore respectfully request that the rejections of independent claims 1 & 11 and also the dependent claims be reconsidered and withdrawn.

Conclusion

For all the foregoing reasons it is believed that all of the claims of the application are in condition for allowance and their passage to issue is earnestly solicited. Applicant's attorney urges the Examiner to call to discuss the present response if anything in the present response is unclear or unpersuasive.

Respectfully submitted,

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